

Results of Sandia National Laboratories Grid- Tied Inverter Testing

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RESULTS OF SANDIA NATIONAL LABORATORIES GRID-TIED INVERTER TESTING

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ABSTRACT: This paper proposes a definition for a “Non-Islanding Inverter”. This paper also presents methods that can be used to implement such an inverter, along with references to prior work on the subject. Justification for the definition is provided on both a theoretical basis and results from tests conducted at Sandia National Laboratories and Ascension Technology, Inc.

Keywords: Islanding – 1: Grid-Connected – 2: Inverter – 3.

1. PREVIOUS TESTING AT SANDIA

During the summer of 1997 Sandia conducted a series of tests to investigate islanding of multiple inverters on a single 120-V ac circuit. It was found that for $P_{\text{generation}}/P_{\text{load}}$ ratios in the range of .8 to 1.2 the inverters frequently islanded for more than the minimum 2 seconds (times > 30 seconds were observed) that was required by some utility customers. It was also observed that the presence of a transformer in the islanded circuit resulted in a shorter islanding times (disconnect times of < .5 seconds) because the transformer requires nonlinear magnetizing current that most inverters could not supply.

The conclusions drawn from these tests were

- multiple inverters on a single 120 V ac circuit were not disconnecting quickly enough,
- the presence of a distribution transformer resulted in quicker disconnect,
- future tests should include other than purely resistive loads, so that a worst-case islanding conditions could be determined,
- the use of multiple inverters utilizing different anti-islanding techniques increased islanding times.

Sandia initiated a working group composed of US inverter manufacturers to address these issues, and sponsored the development of a new approach to prevent islanding through Ascension Technology, Inc. The results of this work are discussed below.

2. DEFINITIONS

2.1 Non-Islanding Inverter

A Non-Islanding Inverter is designed for utility interactive operation. In addition to over/under voltage and over/under frequency trip set points, this inverter includes

the means to ensure unstable operation when the utility is not present. Under normal operating conditions, these inverters will not maintain an island condition. They should be designed so that their active methods are suitable for large numbers of units installed on utility distribution systems and so that their anti-islanding methods do not interact with each under normal operating conditions. A Non-Islanding Inverter meets the test for Non-Islanding Inverters defined below.

2.2 Normal Operating Conditions (NOC)

A section of a utility distribution system that has been disconnected from the rest of the utility is called an island. That island only consists of non-islanding inverters or other equivalent sources of generation and loads. Voltage source inverters or synchronous generators normally will not meet the definitions of a Non-Islanding Inverter. The total aggregate load present in the islanded section is modeled as a parallel RLC circuit, based upon the fundamental components of voltage and current.

An RLC circuit has a characteristic frequency, sometimes called resonant frequency, f_{res} . An RLC circuit also has a quality factor Q_{res} , or damping factor z , which is a measure of whether the circuit is highly resonant or well damped:

$$f_{\text{res}} = 1 / (2\pi(LC))^{1/2} \quad (1)$$

$$Q_{\text{res}} = 1 / (2z) = R(C/L)^{1/2} \quad (2)$$

The authors propose that normal operating conditions (NOC) be defined as any island, or utility load in which the following is true:

$$Q_{\text{res}} < 5 \quad (z > 0.10) \quad \text{when} \quad UF \leq f_{\text{res}} \leq OF \quad (3)$$

$$Q_{\text{res}} = \text{any value when } f_{\text{res}} < UF \text{ or } f_{\text{res}} > OF.$$

OF and UF are the over and under frequency trip set points. The values of 59.5 and 60.5 Hz are being considered for use in the United States in IEEE P929 [1], compared with the present settings in IEEE 929 of 59 and

61 Hz. Equations (1) and (2) can be rewritten in terms of real load, P in kW, inductive load $KVAR_L$, and capacitive load $KVAR_C$. The variable, f_m , is the frequency at which $KVAR_L$ and $KVAR_C$ were measured, typically 60.00 Hz.

$$Q_{res} = (KVAR_L * KVAR_C)^{1/2} / P \quad (4)$$

$$f_{res} = f_m (KVAR_L / KVAR_C)^{1/2} \quad (5)$$

It takes five times as much reactance versus real power to exceed a Q_{res} of 5.0. In addition, the inductive reactance and capacitive reactance must be matched to within 1.65%. Real power being generated must be roughly matched to the real load in the island as well. It seems impractical that the aggregate load in an island would ever exceed NOC, let alone meet conditions likely for a run-on condition to occur in an island. Therefore inverters that meet the definition of Non-Islanding Inverter, should be considered to provide sufficient islanding protection. Equations (4) and (5) above may be used by utility engineers to determine if any feeder or section of a feeder operates outside of NOC.

2.3 A Non-Islanding Inverter Test

The Tests for Non-Islanding Inverters include all functions required in a Non-Islanding Inverter. They include verification that the over and under voltage and frequency trip set points operate according to national standard requirements or local utility requirements, e.g., IEEE 929. The inverter must be tested with an RLC load where $Q_{res} \gg 5$ when $UF < f_{res} < OF$.

To perform this test, connect an inductive load to the test circuit so that the inductive VARs are equal to five times the real load. Then adjust capacitance so that both the real and reactive power at the point of disconnect is zeroed out to within 1.0 % of the real power of the load in kVA. Under this abnormal loading condition, the average time to trip may not exceed the time specified in the interconnect standard. This test should be conducted ten (10) times to ensure proper operation.

This test may still be conducted if the inverter is designed to operate at a fixed (not variable) power factor other than unity. Voltage source inverters, or inverters which adjust reactive power output to stabilize frequency, such as stand alone 4 quadrant inverters, will probably not pass this test.

3. A NON-ISLANDING INVERTER METHOD

3.1 Sandia Frequency Shift (SFS)

The frequency-shift method, developed for this program, is an accelerated frequency drift with positive feedback. The positive feedback in the frequency control makes the island frequency unstable when there are no other mechanisms present to regulate island frequency. When the utility or other generators that control frequency are connected, the SFS unstable frequency controls do not affect frequency. When the utility is disconnected, the SFS method causes frequency to shift out of the frequency trip set points, causing the inverter to shut down.

When the island frequency starts to move up compared to average frequency, the reference frequency of the inverter moves up at a faster rate. When the island frequency moves down compared to average frequency, the reference frequency of the inverter moves down at a faster rate. In order to prevent out of phase operation

between the inverter output and the utility during operation in the normal frequency window, the inverter reference signal is reset at every zero crossing of the voltage waveform. This method was implemented digitally in the inverter firmware.

3.2 Sandia Voltage Shift (SVS)

The voltage shift method is similar to the SFS method. Amplitude of the output current waveform is adjusted in response to utility voltage. When voltage increases, output current is increased. When voltage decreases, output current is decreased. The control signal is based upon the difference between average voltage as measured by an IIR (infinite impulse response) filter and cycle by cycle measurements of voltage. During normal operation, there will be some fluctuation of the utility voltage. If the positive feedback gain is chosen as 2.0, then when the utility voltage fluctuates by 1%, the output current will fluctuate by 2%. This method was suggested by two of the U.S. inverter manufacturers.[2][3].

3.3 Voltage and Frequency Trip Set Points

The voltage and frequency trip set points in Table I were used during all of the tests. In the final implementation tested, these trip set points were the only means for automatic shut down of the inverters.

Table I - Trip Set Points		
	Set Point	Time to Operate (cycles)
Frequency	> 63.0 Hz	1/2
	> 60.5 Hz	5
	< 59.5 Hz	5
	< 57.0 Hz	1/2
Voltage	> 145 V	1
	> 132 V	100
	< 110 V	100
	< 60 V	5
	< 30 V	1

3.4 Unstable Frequency Trip

Additional means to shut down the inverter may be implemented to supplement the voltage and frequency trip set points. An unstable frequency trip method complements the SFS method. In many but not all tests, the SFS method appears to cause frequency to fluctuate more than normal. These frequency fluctuations occur during the island before the frequency has had time to move outside the frequency limits listed above.

In initial tests a df/dt computation was implemented on a cycle by cycle basis. The absolute value of frequency fluctuation was computed and then filtered with a digital IIR filter. The result was compared with a frequency rate of change of 0.09 Hz/cycle. The initial tests proved very effective, in most cases shutting down the inverter in fewer than 20 cycles. However, there appeared to be nuisance tripping due to the highly sensitive setting.

It is likely that some form of df/dt trip can be successfully implemented to complement the SFS method. Optimization of the IIR filter constants and the trip set point could be performed. This optimization is left for a

later time. The present work concentrated on the development and testing of the SFS and SVS methods.

3.5 Prior Inverter Designs

The first inverter to incorporate islanding protection similar to SFS that the authors are aware of, was American Power Conversion Corporation's (APCC) SunSine2000[4]. The APCC inverter used a compensation circuit in the phase response filter portion of the phase lock loop. Far away from 60 Hz, the phase lock loop was stable, and allowed the unit to find and lock onto a 60 Hz voltage. At these frequencies an out-of-frequency trip caused utility disconnect. At frequencies closer to 60 Hz, positive feedback in the frequency control of the phase lock loop makes operation in an island unstable. Other work has been reported that shows excellent results in using similar methods with unstable frequency control [5] [6].

4. TEST RESULTS

4.1 The Significance of Magnetic Components

Before the inverter test results are presented, an important point must be made about magnetic components and their use in islanding testing. Magnetic components such as inductors, transformers and induction motors generally use core materials that are non-linear. In practice, most magnetic components are operated at voltages near their voltage ratings.

Measurements have been made on inductors and transformers to determine the extent to which the measured linearized inductance varied as a function of voltage. The effective inductance of the components tested was found to be highly non-linear in the region of their voltage ratings. The inductors were found to be more ideal (linear) when tested at voltages less than their rated voltage.

The reason this is significant is that in an island, if the voltage increases, then the effective inductance of the magnetic components in the loads will decrease. This will cause the island frequency to increase, so much so that the inverters will shut down on a frequency trip before a voltage trip is reached.

If magnetic components are used in islanding testing at voltages less than their rating, they may behave more like ideal inductors. This may result in longer island times than would occur from operating conditions in the field.

4.2 Defining a Motor Load

A single-phase induction motor with flywheel (grinding wheels) was used in the motor load tests. Capacitance was added to the motor circuit to correct the power-factor to unity. Real power was matched by adding resistance to the motor circuit or by controlling the inverter output power to match the losses in the motor.

The degree to which a motor load will cause an inverter to run-on after disconnect of the utility depends upon one thing: namely, the ratio of rotational kinetic energy stored in the motor to the energy loss per cycle of the motor. The energy losses are due to electrical losses and mechanical losses, such as friction. If there are other resistive loads attached to the same circuit, then they will also help to dissipate the stored energy in the motor.

Measuring the number of cycles (time) it takes for the voltage across the motor to drop by $\frac{1}{2}$ is one means of

quantifying the ratio of stored energy to power dissipation. This measurement is made with a power factor corrected motor and no resistive load. The number of cycles is measured with the inverter disabled and is measured from the time the power is disconnected. The authors propose that when motor loads are used in islanding tests, this measurement should be provided, since it is needed to properly specify the test setup. The number is needed so that subsequent test conditions can be reasonably compared. Although the authors do not bound this number, they do identify the numbers used in their tests.

4.3 Worst Case Loads

During the preliminary testing while the anti-islanding methods were being developed, two types of loads were found to result in the longest islanding times. These loads were RLC loads that had a resonant frequency of $60 \pm \frac{1}{2}$ Hz and loads that contained induction motor loads with flywheels and capacitive VAR correction.

Preliminary tests included a wide range of generation to load ratios and load conditions. During the final testing, efforts concentrated on worst case load testing only.

4.4 Single Inverter Tests at Ascension Technology

Tests conducted at Ascension Technology were conducted with a single modified SunSine™300 inverter. A dc power supply was used to provide controlled input power. Since the tests were conducted in the manufacturer's facilities, it was possible to control the inverter through a diagnostics interface. This allowed a much faster test cycle time than is possible in field testing. The firmware installed was version 1.46 of the SunSine™300; it utilized the SFS and SVS methods for anti-islanding.

4.4.1 RLC Loads

The data in the following charts indicates the trip time for a series of tests. For example, in Figure 1, each line shows the change in voltage as a function of cycles (time) with the disconnect time occurring at the point where the line ends. The variable is the P_{gen} .

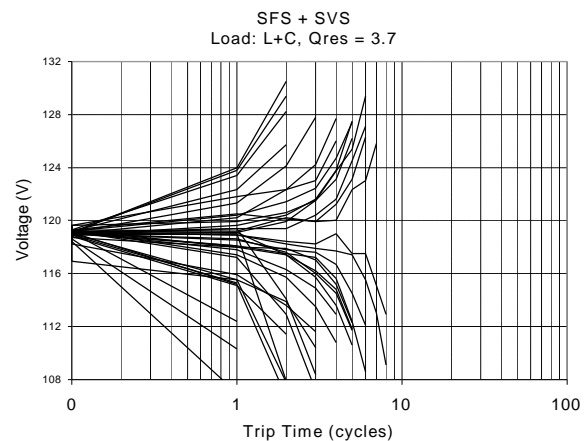


Figure 1. RLC load, voltage trajectories.

The goal of the RLC tests was to achieve the highest possible resonant load. For this set of tests, only inductance and capacitance were used for the load. The resistance in these tests comes from the losses in the inductor. In this case, $Q_{res} = 3.7$. During the tests, the

inverter was operated over a range of power levels to get a range of generation/load ratios. Figure 1 shows the voltage trajectories for the various tests and Figure 2 shows the frequency trajectories. Note that the voltage and frequency are unstable and not able to sustain an island. In this set of tests the inverter shut down within 10 cycles due to frequency trips.

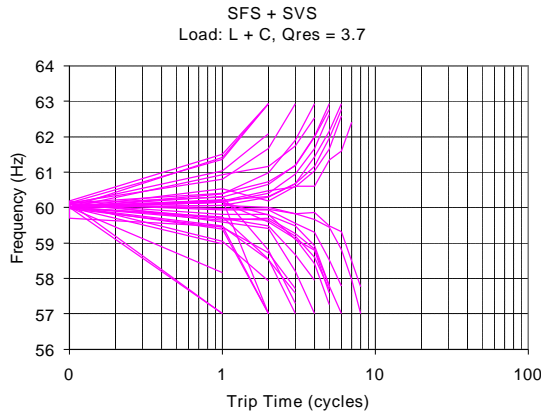


Figure 2. RLC load, frequency trajectories

The tests presented were the worst case tests. Other RLC load combinations were tested, but due to space limitations are not presented here.

4.4.2 Induction Motor Load Test

A ½-hp induction motor with grinding wheels attached was used for the next series of tests. Capacitance, 261 VAR_{S_C}, was added to correct the power factor of the motor to 1.00. No additional resistance was added to the test circuit, but the no-load losses of the motor were 119 watts.

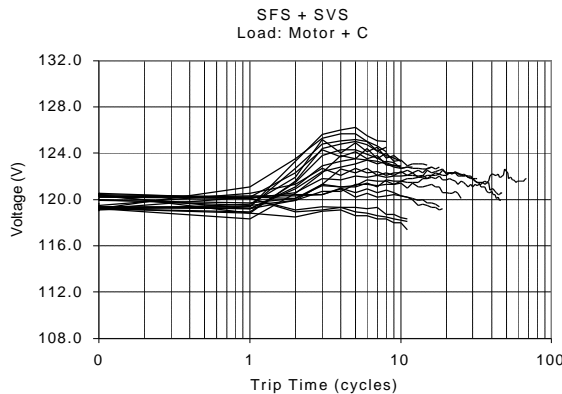


Figure 3. Voltage trajectories for power-factor corrected motor

Again, a range of inverter power levels was used to achieve a range of generation/load ratios. Figures 3 and 4 show the voltage and frequency trajectories of these tests. In these tests, no island exceeded 70 cycles and all anti-island shutdown actions were due to frequency trips. The power-factor corrected motor voltage dropped by ½ in 42 cycles after disconnect of all ac power.

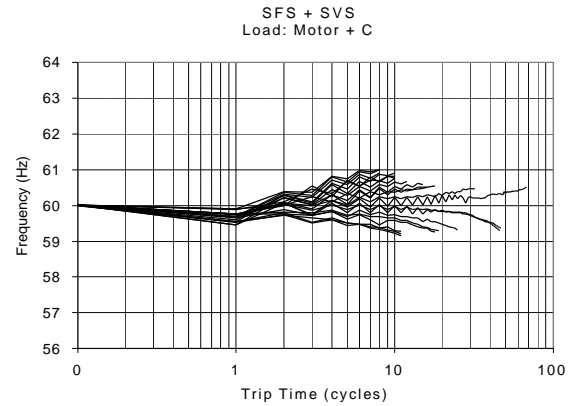


Figure 4. Frequency trajectories for power factor corrected motor

4.5 Test Results from Sandia National Laboratories

4.5.1 Configuration.

Three of the SunSine™ 300 AC Modules were connected in parallel with various loads on an outdoor field array for the evaluation of the SVS/SFS anti-islanding technology. The circuit configuration is shown in Figure 5. The various loads were configured, as required, for each test and included R, RL, RLC, RC, motor, and motors with capacitive VAR compensation. The ½-hp induction motor load included a flywheel, to maximize the back emf. Parameters varied included power factor, $P_{\text{generation}}/P_{\text{load}}$, and Q_{res} . One of the two contactors shown was used to interrupt the utility power. The location of the contactor used for a test was important because of the nonlinearity of the magnetizing currents in the transformer. When the primary contactor was opened, the distribution transformer remained in the islanded circuit. Since the inverters could not supply harmonics of 60 Hz, the presence of the transformer aided a rapid inverter disconnect.

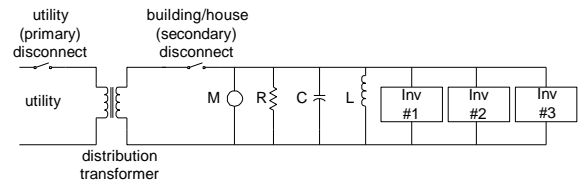


Figure 5: Diagram of circuit configuration

The test loads were selected based on input from previous testing at SNL and input from industry and utility sources. The “distribution transformer” used for those tests that included a primary side disconnect was unusually small (2 kVA) for a distribution transformer; however, that size was used to avoid overwhelming the three 300-watt, module-scale inverters. This approach resulted from a belief that two 4-kW inverters connected to a 15-kW distribution transformer would operate in a similar manner.

Initially the value of C in the RLC circuit was fixed at 301 micro-farads and L was selected to provide 60-Hz resonance. The value of R was then sized to dissipate power equal to that produced by the three parallel inverters. Matching inverter power output with the resistance was a necessary condition for islanding. Since the value of R also determines Q_{res} , it follows that in order to obtain high Q_{res} , the inverters were required to operate at

low power (Table II). Thus the circuit could be islanded only for particular combinations of inverter output power and RLC.

Q_{res}	Power (watts)
2	839
5	328
10	164
20	81

Table II: Dissipation power of R that produces Q_{res} for a fixed value of $C = 301 \mu F$

4.5.2 Test Results.

Two sets of data are presented. The first data set (Table III, column 2) was the result of extensive testing of the SFS anti-islanding approach. This was an extensive test series that evaluated a full range of load types. The results of the evaluation show that the approach was very successful for all cases with the exception of RLC loads resonant at 60 Hz. The run-on time is related to the circuit Q_{res} , with run-on times exceeding 6 cycles (approximately 100 milliseconds) for a Q_{res} in excess of 1.5. For $1.5 < Q_{res} < 7$, the inverter shut down in less than .5 seconds. For two of the higher Q_{res} cases (Q_{res} of 8 and 11), the circuit islanded until operator intervention

Load	SFS with df/dt	SFS & SVS
R	.068	no data
RL	.028	no data
RC	.036	no data
RLC	Island*, $Q=11$.32, $Q=7$, $301 \mu F$
motor	.228, $C=67 \mu F$.53, $C= 67 \mu F$
RLC	no data	.78, $Q>8$, $641 \mu F$

*operator intervention required

Table III: Islanding times in seconds

The second set of data (Table III, column 3) includes both the SFS and the SVS anti-islanding methods. This series of data was limited to the previously identified worst cases, RLC and a ½-hp induction motor load (with flywheel). The power-factor-corrected motor voltage dropped by ½ in 55 cycles after disconnect of all ac power. This series of tests shows that the islanding associated with RLC resonance has been eliminated; the longest time was .32 seconds for a $Q_{res} = 7$ case.

The last row of data results from doubling the available capacitance and hence increasing the allowable power output from the inverters for a specific value of Q_{res} . While this doubled the islanding time to .78 seconds, the islanding time is still not lengthy and the Q_{res} of 8 is very high.

Recalling the comparison to two 4-kW inverters connected to a 15-kVA transformer, it is clear that power matching any significant power output of these larger inverters would require a low value of resistance and thus a very low Q_{res} circuit. The conditions for which the inverters were found to island for the SVS/SFS anti-

islanding approach are unlikely to occur in normal distribution circuits where Q_{res} is generally less than 5.

5. CONCLUSIONS

The combination of SVS and SFS were shown to be sufficient to achieve a Non-Islanding Inverter.

SVS and SFS are likely to work with high penetrations of distributed generators. They do not require synchronization between inverters to operate. They do not perform active perturbations on the utility system that can be undesirable or unworkable in high penetrations. Other active methods that try to perturb the utility and measure a coincident change in voltage or frequency will not work in high penetrations unless the perturbations are synchronized.

The SVS and SFS methods have been easy to implement. The only modifications necessary to implement them were changes in firmware in an existing inverter design. No changes to the hardware were required. This may not be true for all inverter designs.

Additional utility input is needed to determine an appropriate value of Q_{res} in the definition of normal operating conditions (NOC). The results presented here are far superior to results of other anti-islanding tests conducted over the last 18 months both at Ascension Technology, Inc. and at Sandia National Labs.

This work was supported by a consensus of U.S. inverter manufacturers. Although not guaranteed, it is likely that the results of this work will move the industry toward a defacto standard for anti-islanding in the United States. It is hoped that by sharing these results, similar methods would be considered in the international community.

6. REFERENCES

- [1] ANSI/IEEE Draft Standard P929-1998, Draft 5, Recommended Practice for Utility Interface of Photovoltaic (PV) Systems.
- [2] R. Wills, Advanced Energy Systems, discussions at Soltech 1998 with R. Bonn and G Kern.
- [3] C. Freitas, Trace Engineering, discussions at Soltech 1998 with R. Bonn and G Kern.
- [4] O. Wasynczuk, P.C. Krause, *Computer Modeling of the American Power Conversion Corporation Photovoltaic Power Conditioning System*, Sandia National Labs Contractor Report SAND87-7006, March 1987.
- [5] T. Ambo, "Islanding prevention by Slip Mode Frequency Shift," IEA-PVPS-Task V, *Proceedings of the Grid Interconnection of Photovoltaic Systems Workshop*, Zurich, September 1997.
- [6] Chihiro Okado, *Protection Device for Stopping Operation of an Inverter*, assignee K.K. Toshiba, U.S. Patent No. 5,493,485 Feb 20, 1996.

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